[Method of dividing a semiconductor integrated circuit pattern]

Abstract of Disclosure

A method of dividing a semiconductor integrated circuit pattern. The pattern has a plurality of cells with the same shape and a polygonal planar positioned between each cell, the polygonal planar has two parallel horizontal edges and a plurality of vertexes.The method includes depicting a division line to divide the polygonal planar positioned between each cell into a plurality of unit figures. The division line begins along a horizontal edge of the polygonal planar, and when meeting with a vertex, the division line extends a vertical line segment from the horizontal edge to another horizontal edge.

Figures